

WHAT IS CLAIMED IS:

1 1. A dynamic logic circuit having an output and a complementary output
2 comprising:

3 a first electronic switch having an input terminal coupled to a clock signal, a
4 first terminal coupled to a positive power supply voltage and a second terminal
5 coupled to a dynamic node of said dynamic logic circuit, wherein said dynamic node
6 is coupled to said positive power supply voltage in response to a first logic state of a
7 clock signal and isolated from said positive power supply voltage in response to a
8 second logic state of said clock signal;

9 a logic tree having a plurality of logic inputs, a positive tree terminal coupled
10 to said dynamic node and a negative tree terminal, wherein said positive tree terminal
11 is coupled to said negative tree terminal in response to first logic states of said
12 plurality of logic inputs and isolated from said negative tree terminal in response to
13 second logic states of said plurality of logic inputs;

14 a second electronic switch having an input coupled to said clock signal, a first
15 terminal coupled to said negative tree terminal and second terminal coupled to a
16 negative power supply voltage, wherein said negative tree terminal is coupled to said
17 negative power supply voltage in response to said second logic state of a clock signal
18 and isolated from said positive power supply voltage in response to a first logic state
19 of said clock signal;

20 a keeper circuit having a power supply terminal coupled to a positive power
21 supply voltage, a keeper output coupled to said dynamic node, a keeper input coupled
22 to said complementary output, wherein said keeper circuit reinforces a first logic state
23 on said dynamic node only when said dynamic node evaluates to a logic one and said
24 output transitions to a logic zero; and

25 static output logic circuitry having an input coupled to said dynamic node, a
26 static output generating said output, an inverted static output generating said
27 complementary output, and an enable terminal, wherein said enable terminal is
28 coupled to said negative power supply voltage by a third electronic switch in response
29 to said second logic state of said clock signal and by a fourth electronic switch in
30 response to said second logic state of said complementary output.

1 2. The dynamic logic circuit of claim 1, wherein said keeper circuit comprises a
2 P channel field effect transistor (PFET) having a gate terminal coupled to said
3 complementary output, a source terminal coupled to said power supply terminal and a
4 drain terminal coupled to said keeper output.

1 3. The dynamic logic circuit of claim 1, wherein said complementary output is
2 generated by inverting said output using an inverter logic gate.

1 4. A logic device comprising:

2 a plurality of dynamic logic circuits wherein each of said dynamic logic
3 circuits has a first electronic switch having an input terminal coupled to a clock
4 signal, a first terminal coupled to a positive power supply voltage and a second
5 terminal coupled to a dynamic node of said dynamic logic circuit, wherein said
6 dynamic node is coupled to said positive power supply voltage in response to a first
7 logic state of a clock signal and isolated from said positive power supply voltage in
8 response to a second logic state of said clock signal, a logic tree having a plurality of
9 logic inputs, a positive tree terminal coupled to said dynamic node and a negative tree
10 terminal, wherein said positive tree terminal is coupled to said negative tree terminal
11 in response to first logic states of said plurality of logic inputs and isolated from said
12 negative tree terminal in response to second logic states of said plurality of logic
13 inputs, a second electronic switch having an input coupled to said clock signal, a first
14 terminal coupled to said negative tree terminal and second terminal coupled to a
15 negative power supply voltage, wherein said negative tree terminal is coupled to said
16 negative power supply voltage in response to said second logic state of a clock signal
17 and isolated from said positive power supply voltage in response to a first logic state
18 of said clock signal, a keeper circuit having a power supply terminal coupled to a
19 positive power supply voltage, a keeper output coupled to said dynamic node, a
20 keeper input coupled to said complementary output, wherein said keeper circuit
21 reinforces a first logic state on said dynamic node only when said dynamic node
22 evaluates to a logic one and said output transitions to a logic zero, and static output
23 logic circuitry having an input coupled to said dynamic node, a static output
24 generating said output, an inverted static output generating said complementary
25 output, and an enable terminal, wherein said enable terminal is coupled to said
26 negative power supply voltage by a third electronic switch in response to said second

27 logic state of said clock signal and by a fourth electronic switch in response to said
28 second logic state of said complementary output.

1 5. The dynamic logic circuit of claim 4, wherein said keeper circuit comprises a
2 P channel field effect transistor (PFET) having a gate terminal coupled to said
3 complementary output, a source terminal coupled to said power supply terminal and a
4 drain terminal coupled to said keeper output.

1 6. The dynamic logic circuit of claim 4, wherein said complementary output is
2 generated by inverting said output using an inverter logic gate.

1 7. A data processing system comprising:
2 a central processing unit (CPU); and
3 a memory operable for communicating instructions and operand data to said
4 CPU, wherein said CPU includes a logic system having a logic device, said logic
5 device including a plurality of dynamic logic circuits wherein each of said dynamic
6 logic circuits has a first electronic switch having an input terminal coupled to a clock
7 signal, a first terminal coupled to a positive power supply voltage and a second
8 terminal coupled to a dynamic node of said dynamic logic circuit, wherein said
9 dynamic node is coupled to said positive power supply voltage in response to a first
10 logic state of a clock signal and isolated from said positive power supply voltage in
11 response to a second logic state of said clock signal, a logic tree having a plurality of
12 logic inputs, a positive tree terminal coupled to said dynamic node and a negative tree
13 terminal, wherein said positive tree terminal is coupled to said negative tree terminal
14 in response to first logic states of said plurality of logic inputs and isolated from said
15 negative tree terminal in response to second logic states of said plurality of logic
16 inputs, a second electronic switch having an input coupled to said clock signal, a first
17 terminal coupled to said negative tree terminal and second terminal coupled to a
18 negative power supply voltage, wherein said negative tree terminal is coupled to said
19 negative power supply voltage in response to said second logic state of a clock signal
20 and is isolated from said positive power supply voltage in response to a first logic
21 state of said clock signal, a keeper circuit having a power supply terminal coupled to
22 a positive power supply voltage, a keeper output coupled to said dynamic node, a
23 keeper input coupled to said complementary output, wherein said keeper circuit
24 reinforces a first logic state on said dynamic node only when said dynamic node
25 evaluates to a logic one and said output transitions to a logic zero, and static output
26 logic circuitry having an input coupled to said dynamic node, a static output

27 generating said output, an inverted static output generating said complementary
28 output, and an enable terminal, wherein said enable terminal is coupled to said
29 negative power supply voltage by a third electronic switch in response to said second
30 logic state of said clock signal and by a fourth electronic switch in response to said
31 second logic state of said complementary output.

1 8. The data processing system of claim 7 wherein said keeper circuit comprises a
2 P channel field effect transistor (PFET) having a gate terminal coupled to said
3 complementary output, a source terminal coupled to said power supply terminal and a
4 drain terminal coupled to said keeper output.

1 9. The data processing system of claim 7 wherein said complementary output is
2 generated by inverting said output using an inverter logic gate.

1 10. A dynamic logic circuit having an output and a complementary output
2 comprising:

3 a dynamic node;

4 precharge circuitry coupled to said dynamic for precharging the dynamic node
5 to a logic one during a precharge cycle of a clock signal;

6 a logic tree coupled to said dynamic node for evaluating said dynamic node to
7 a logic one or a logic zero in response to combinations of logic states of plurality of
8 logic inputs coupled to said logic tree during an evaluation cycle of said clock signal;

9 static logic circuitry for latching a logic state of said dynamic node and
10 holding said logic state during said precharge cycle of said clock signal, wherein said
11 static logic circuitry generates said output and said complementary output; and

12 a keeper circuit having a power supply terminal coupled to a power supply
13 voltage, a keeper input coupled to said complementary output and a keeper output
14 coupled to said dynamic node, wherein said keeper output reinforces a first logic state
15 of said dynamic node only when said dynamic node evaluates to a logic one and said
16 output transitions to a logic zero.

1 11. The dynamic logic circuit of claim 10, wherein said keeper circuit comprises a
2 P channel field effect transistor (PFET) having a gate terminal coupled to said
3 complementary output, a source terminal coupled to said power supply terminal and a
4 drain terminal coupled to said keeper output.